DECLARATION OF OSWIN SCHREIBER UNDER 37 CFR §1.132

I, Oswin Schreiber, Ph.D., hereby declare as follows:

1. My residence address is 12949 Angosto Way, San Diego, CA 92128.

2. My degrees include:

University of Mainz, PhD in Physics 1985; and

University of Mainz, Master in Physics 1980.

3. A list of some of my publications is enclosed as Attachment D.

4. From 1985 until 1987, I worked at Toshiba LTD, in Munich, with the Sales Department.

5. From 1987 until 1988, I worked at Siemens, in Munich, as the Product Marketing Manager of Optical Data Links.

6. From 1988 until 2000, I worked at AT&T ME/Lucent Microelectronics, in Munich. My responsibilities included Marketing Manager for High Speed Physical Layer Devices, Distributor Manager, and Sales Engineer.

7. Since September 1st, 2000 I have been employed by Applied Micro Circuits Corp. (AMCC), 6290 Sequence Drive, San Diego, CA 92121. My title at AMCC is Senior Product Marketing Scientist. My

responsibilities Product Marketing functions, coordinating R&D efforts, leading new product ideas to marketable products representing AMCC's products in the optical market space, and publishing articles.

8. I have read the claims for the patent application in question, Castagnozzi et al., Serial Number 10/020,426 (the Applicant). I have read the relevant parts of the Office Action dated December 9, 2004, where 17, 33, and 35 have been rejected as obvious with respect to Andresen (US 3,670,304) and Abe (US 5,781,588). In summary, it is my opinion that neither of the cited references, even when combined makes the invention of claims 17, 33, or 35 obvious.

9. In claims 17, 33, and 35, and as shown in Fig 3, the Applicant recites two claims elements: a multi-threshold decision circuit and a non-causal circuit. Claim 35 includes the additional claim element of an FEC circuit. The multi-threshold decision circuit accepts an input and supplies a plurality of bit estimates for each input symbol. That is, the incoming data symbol is simultaneously compared to several different thresholds. The non-causal circuit accepts these bit estimates and compares one of the bit estimates (the first bit estimate) to bit decisions for other clock cycles. In response to the comparison, the non-causal circuit generates the current (first) clock cycle bit value.

With respect to claim 35, the FEC circuit accepts the bit values, performs FEC corrections, and uses these corrections to adjust the threshold levels of the multi-threshold decision circuit, to minimize the number of FEC corrections that are required.

10. Andresen describes a magnetic tape reading device that accepts an analog signal with a non-predetermined amplitude. Andresen compares the input to thresholds for the purpose of creating a hard-limited

digital input from the analog signal. Threshold decisions are made at amplitude sensor 14, and OR gate 18 to create the hard-limited signal on line 27 of Fig. 1. This signal is fed to the data detector for the purpose of generating data pulses, clock pulses, and as an input to the feedback circuitry that is used to generate the limiter threshold values.

11. There are several differences between Andresen and claims 17, 33, and 35. The purposes of the inventions are different. Andresen is primarily concerned with creating digital data from a magnetic tape analog input signal. The problem to be solved by Andresen is that the analog input voltage levels fluctuate. That is, Andresen is trying to generate accurate digital values from a binary values embedded in an analog signal. The purpose of the Applicant's invention is to generate accurate digital values by eliminating the interference resulting from the voltage levels of neighboring symbols.

Generally, Andresen uses a feedback circuit to adjust the limiter threshold values. Simultaneously, Andresen converts the limited signal to impulse (narrow) pulses, decouples the impulse pulses from phase changes, generates a clock signal, and in response to clock and impulse pulses, generates data pulses. In contrast, the Applicant chooses not to hard-limit the input signal, but rather creates multiple bit estimates of what an input symbol might represent using parallel threshold comparators. The Applicant's non-causal circuit, knowing the sequence of bit decisions, selects a threshold value, and therefore a bit estimate, that optimally accounts for voltage error inherent in the sequence. For example, if the previous and subsequent data values are both "1", the non-causal circuit compensates for the effect of a generally higher voltage level at the time of the current clock bit decision.

12. There are profound differences between Andresen and the Applicant's circuitry. First, Andresen does not create several bit estimates by comparing an input symbol to various threshold levels. In the Applicant's invention, the bit estimates are a preliminary decision made as to the binary value of the input symbol. That is, each input symbol generates a plurality of parallel binary values, either a "1" or a "0". Each estimate is a decision as the whether the input symbol is a "1" or "0". Andresen's limited signal is not a decision of the input symbol's binary value, although the limited signal may closely track the data value that is ultimately made further on in the process. Rather, the limited signal is simply a processed version of the input signal. A high voltage input (see "A", Fig. 2) is emphasized (limited) to be a maximum voltage (see "E", Fig. 2). Likewise, a low voltage is processed (limited) to be a minimum voltage. It should be noted that when the analog input amplitude is too small, no processing is performed, and the analog input is passed on line 27 unprocessed. In this circumstance, Andresen's limiter does not create a signal that even looks like digital data. If Andresen's limited signal (line 27) were to be considered to be an estimate, then the estimates are only made in some circumstances, when the input signal amplitudes are large enough. The fact that Andresen's hard-limited signal looks like a digital signal (in some circumstances) should not be confused with the fact that Andresen's circuitry makes no determination of the binary symbol values on line 27. The binary symbol value determinations are made later in the process, in Andresen's data detector.

Further, the hard-limiting process does not provide a plurality of bit estimates for each input symbol, but rather only a single signal per input symbol (per tape track). Line 72 (Fig. 3) shows that there is only a single output for each tape track. That is, there is only a single hard-limited signal

for each input data stream. Thus, Andresen does not describe a circuit or combination of circuits that perform the function of the Applicant's multi-threshold decision circuit.

13. Second, Andresen does not perform a non-causal analysis. Andresen never makes a bit decision dependent based upon the bit values decisions made in other clock cycles. Thus, Andresen does not describe a circuit, or combination of circuits that perform the function of the Applicant's non-causal circuit. The Office Action states that Andresen's data detector functions as a non-causal circuit. Andresen's data detector might be said to generate a current clock cycle bit value in response to the hard-limited signal input. However, this decision is made without the consideration of bit decisions made in other clock cycles. As I mentioned above, Andresen converts the hard-limited signal to impulse (narrow) pulses, decouples the impulse pulses from phase changes, generates a clock signal, and in response to clock and impulse pulses, generates data pulses. The circuit has no inputs to accept decision data made for other clock periods. The Office Action, at the beginning of page 6, states that a current bit estimate D is compared to "reference decisions R1 and R2 made across a plurality of clock cycles; Note; bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles". While I am not entirely sure of the Examiner's point, it is clear that R1 and R2 are not bit values that are determined for non-current clock cycles. Rather, R1 and R2 are shown to be constant amplitude waveforms in Fig. 3. Andresen describes R1 and R2 as reference levels (col. 8, ln. 46-49).

14. Abe describes a variety of FSK demodulation circuits. As is conventional with such circuits, the carrier signal is amplified if it is close to the noise floor, and attenuated (amplified to a lesser degree) if the carrier

signal or in-band spurious signals are relatively large in signal strength. Also, as is conventional, the input signal is down -converted to an IF band, further down -converted to baseband to recover the FM (baseband) spectrum. Then, the FM spectrum is converted to a digital signal. The binary data can be represented in return-to-zero (RZ), return-to-bias (RB), NRZ or other formats. The digital data is recovered using a threshold (bit-state) detector. In one embodiment mentioned in the Office Action (Fig. 37), the point of novelty appears to be that an analysis of the BER can be used to adjust the thresholds used by the bit-state detector to make bit decisions.

15. There are several differences between the Abe invention and the invention of claims 17, 33, and 35. As with Andresen, the differences primarily stem from the entirely different uses to which the inventions are put. Abe's bit-state detector must compensate for errors associated with the input carrier frequency, errors in the LO frequency, variations in input power, the generation of in-band mixer spurs, and errors associated with the demodulation frequency (typically a phase-locked loop). All these potential errors contribute to the digital signal that is detected by the bit-state detector. While Abe does describe the use of BER data to "tune" the bit-state detector thresholds, Abe does not describe circuitry that generates a plurality of bit estimates for each input symbol, or perform a non-causal analysis of bit decisions.

16. I have been asked to state whether I, as an expert in the field, would have been motivated to combine the Abe and Andresen inventions. I have summarized the Abe and Andresen circuitry above, and noted distinctions between the prior art references and the claimed invention. However, the differences between the Abe and Andresen inventions are also quite substantial. At the highest level of abstraction, it is unlikely that I

would look to an RF receiver AGC control circuit to make modification to a tape drive reader. I would consider these types of inventions to be in different fields of art, that rarely cross-pollinate, due to the difference in problems being solved. At the lowest level of abstraction, both inventions compare an input signal to a threshold level, and generate a bit decision. These are very common circuit functions. However, the different uses of the comparator circuits mitigate against any kind of combination. Andresen describes the use of a comparison threshold for hard-limiting an analog tape drive input. This limiting circuit appears to have no applicability to Abe's bit-state detector. Abe does not hard-limit the input to his bit-state detector. If the Examiner is correct in stating that there is indeed a motivation to combine there references, then it must be true that there is motivation to combine any two communication devices. If that were true, I see no point in creating a test for motivation to combine.

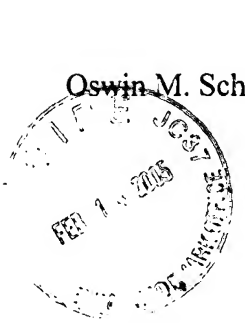
17. I have also been asked to consider whether the combination of the Abe and Andresen inventions would result in all the components of the claimed invention, regardless of whether an expert would have realistically sought to combine these inventions. I have mentioned above that neither the Abe nor the Andresen inventions describe the elements of a multi-threshold circuit, which create a plurality of bit estimates for each input symbol. Further, neither Abe nor Andresen describe a non-causal circuit that accepts the bit estimates and creates a bit value for the current clock cycle in response to comparing the bit estimates to bit decisions made in other clock cycles. Without these two components, the claimed invention cannot be practiced. Thus, even if an expert combined every relevant feature from the Abe and Andresen inventions, the result could not be the Applicant's invention.

18. In summary, my opinion is that the cited prior art does not teach the key aspects of the claimed invention, whether considered separately, or in combination. Further, the combination does not suggest any kind of synergistic leap to the claimed invention, as neither reference even discusses the issue of non-causal analysis, much less a circuit to enable such a function.

19. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United State Code and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

____01/14/05_____ _____

Date Oswin Schreiber



PUBLICATIONS OR OTHER MAJOR MEDIA:

Throughout his career, Dr. Schreiber has authored several vital and germane articles that continue to be extensively used by other leading scientists and researchers in his field (being cited over 330 times). Examples of Dr. Schreiber's authorship of scholarly articles in the field, in professional journals are as follows: (not all listed)

1. Article entitled; "***40-Gbit/s nets call for process shift***," Planet Analog, The EE Times Community (27 Sept. 2004).
2. Article entitled; "***Cost-effectively Designing for 10 Gbit and Beyond in the MAN***," The EE Times (2004).
3. Article entitled; "***OC-768: Jumping Physical Design Hurdles***," The EE Times and CommsDesign (CMP) (29 Aug. 2002).
4. Article entitled; "***40-Gb/s Circuits Built from a 120-GHz f_T SiGe Technology***," The IEE Journal of Solid-State Circuits, Vol. 37, No. 9. (Sept. 2002).
5. Article entitled; "***Diverse Integration a Key Enabler***," The EE Times (06 Aug 2001).
6. Article entitled; "***Optical Communications 40-Gbit/s nets call for process shift***," The Technology Network and The EE Times (13 Apr 2001).
7. Article entitled; "***The Asterix Spectrometer at Lear***," The Nuclear Instruments and Methods in Physics Research, Elsevier Science Publisher A286 (1990) 76-98.
8. Article entitled; "***Antiproton annihilation at rest in nitrogen and deuterium gas***," Physical Review C. Nuclear Physics (Dec. 1989).
9. Article entitled; "***Antiproton-Proton Annihilation at Rest into $\pi+\pi-\pi'$ and $\pi+\pi-\pi$ and the Quark Line Rule***," The Zeitschrift fur Physik C (19 Oct 1989).
10. Article entitled; "***First Observation of K X-Rays from pp Atoms****," The Physics Letters (18 July 1985).
11. Article entitled; "***Protonium Spectroscopy and Identification of P-Wave and S-Wave Initial States of pp Annihilations at Rest with the Asterix Experiment at Lear***," The Physics' at Lear with Low-Entergy Culled Antiprotons, Plenum Publishing Corporation (1984).
12. Article entitled; "***Protonium Spectroscopy and Identification of P-Wave and S-Wave Initial States of pp Annihilations at Rest with the Asterix Experiment at Lear***," The European Organization for Nuclear Research, (01 Oct. 1982).
13. Article entitled; "***A study of pp Interactions at Rest in a H2 Gas Target at Lear***," European Organizaitro for Nuclear Research (29 Aug. 1980).